AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1   1. (Currently amended) An apparatus for detecting errors on a source-
2 synchronous bus, comprising:
3   the source-synchronous bus, wherein the source-synchronous bus includes
4 a plurality of data lines and a clock line;
5   a transmitting mechanism coupled to the source-synchronous bus, wherein
6 the transmitting mechanism is configured to transmit data on the source-
7 synchronous bus;
8   a receiving mechanism coupled to the source-synchronous bus, wherein
9 the receiving mechanism is configured to receive data from the source-
10 synchronous bus;
11   an error detecting mechanism coupled to the receiving mechanism that is
12 configured to detect errors on the source-synchronous bus;
13   a grouping mechanism coupled to the transmitting mechanism that is
14 configured to group data bits into an error group, wherein the grouping
15 mechanism is further configured to skew data bits within the error group across
16 time;
17   a detection code generating mechanism coupled to the grouping
18 mechanism that is configured to generate a detection code for the error group; and
19   the transmitting mechanism that is further configured to transmit the
20 detection code on the source-synchronous bus using a clock cycle other than the
21 clock cycles used for transmitting data bits of the error group, wherein at a given

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| 22 | instant in time each data line in the plurality of data lines carries a data bit from a |
| 23 | different error group; |

wherein each data bit in the error group is transmitted at a different time so

that no two bits associated with the error group are transmitted at the same time;

wherein the receiving mechanism is further configured to deskew the data

bits in the error group; and

wherein the error detecting mechanism can detect errors ~~on the plurality of~~

~~data lines~~in the error group including errors that are caused by an error on the

clock line.

2 (Canceled).

3. (Previously presented) The apparatus of claim 1, wherein the detection
code is a parity bit.

4. (Previously presented) The apparatus of claim 1, wherein the detection
code is an error correcting code.

5 (Canceled).

6. (Previously presented) The apparatus of claim 1, wherein skewing data
bits across time includes delaying a data bit based on a position of the data bit
within the error group.

7. (Previously presented) The apparatus of claim 1, further comprising a
gathering mechanism coupled to the receiving mechanism, wherein the gathering
mechanism is configured to de-skew data bits within the error group.

1   8. (Currently amended) A method for detecting errors on a source-

2   synchronous bus, wherein the source-synchronous bus includes a plurality of data

3   lines and a clock line, the method comprising:

4   grouping data bits into an error group;

5   generating a detection code for the error group;

6   skewing data bits within the error group across time;

7   transmitting data from a source on the source-synchronous bus, wherein

8   each data bit in the error group is transmitted at a different time so that no two bits

9   associated with the error group are transmitted at the same time;~~;~~

10   transmitting the detection code on the source-synchronous bus using a

11   clock cycle other than the clock cycles used for transmitting data bits of the error

12   group<u>, wherein at a given instant in time each data line in the plurality of data</u>

13   <u>lines carries a data bit from a different error group</u>;

14   receiving data at a destination from the source-synchronous bus;

15   <u>deskewing the data bits in the error group;</u> and

16   detecting data errors at the destination, wherein detecting data errors

17   includes detecting errors <u>in the error group </u>that are caused by errors on the clock

18   line.

1   9 (Canceled).

1   10. (Previously presented) The method of claim 8, wherein the detection

2   code is a parity bit.

1   11. (Previously presented) The method of claim 8, wherein the detection

2   code is an error correcting code.

1   12 (Canceled).

1   13. (Previously presented) The method of claim 8, wherein skewing data

2   bits across time includes delaying a data bit based on a position of the data bit

3   within the error group.

1   14. (Previously presented) The method of claim 8, further comprising de-

2   skewing data bits within the error group.

1   15. (Currently amended) A computing system for detecting errors on a

2   source-synchronous bus, comprising:

3   the source-synchronous bus, wherein the source-synchronous bus includes

4   a plurality of data lines and a clock line;

5   a central processing unit coupled to the source-synchronous bus, wherein

6   the central processing unit is configured to transmit data on the source-

7   synchronous bus;

8   a memory unit coupled to the source-synchronous bus, wherein the

9   memory unit is configured to receive data from the source-synchronous bus;

10   an error detecting mechanism coupled to the memory unit that is

11   configured to detect errors on the source-synchronous bus;

12   a grouping mechanism coupled to the transmitting mechanism that is

13   configured to group data bits into an error group, wherein the grouping

14   mechanism is further configured to skew data bits within the error group across

15   time;

16   a detection code generating mechanism coupled to the grouping

17   mechanism that is configured to generate a detection code for the error group; and

18   the transmitting mechanism that is further configured to transmit the

19   detection code on the source-synchronous bus using a clock cycle other than the

20   clock cycles used for transmitting data bits of the error group, wherein each data

21   bit in the error group is transmitted at a different time so that no two bits

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22	associated with the error group are transmitted at the same time, and wherein at a
23	given instant in time each data line in the plurality of data lines carries a data bit
24	from a different error group;;
25	wherein data bits in the error group are transmitted at different times;
26	wherein the memory unit is further configured to deskew the data bits in
27	the error group; and
28	wherein the error detecting mechanism can detect errors on the plurality of
29	data linesin the error group including errors that are caused by an error on the
30	clock line.

1   16 (Canceled).

1   17. (Previously presented) The computing system of claim 15, wherein the
2   detection code is a parity bit.

1   18. (Previously presented) The computing system of claim 15, wherein the
2   detection code is an error correcting code.

1   19 (Canceled).

1   20. (Previously presented) The computing system of claim 15, wherein
2   skewing data bits across time includes delaying a data bit based on a position of
3   the data bit within the error group.

1   21. (Previously presented) The computing system of claim 15, further
2   comprising a gathering mechanism coupled to the memory unit, wherein the
3   gathering mechanism is configured to de-skew data bits within the error group.